Appendix A

Claim (clean version):

1. (currently amended) A network interface, comprising:

a direct memory access unit; and

circuitry to:

receive and transmit network data;

maintain a set of statistics metering operation of the network interface, the set of statistics including at least one selected from the group of: (1) a number of bytes received, and (2) a number of packets received;

periodically initiate direct memory access transfers of the set of statistics to the host processor memory at a periodicity of a time interval value; and

configure said initiation of the direct memory access transfers using a configuration information, by intercepting one or more packets received from said host traveling along a transmit path and determining said configuration information from a payload of said one or more packets, wherein said configuration information comprises said time interval value.

2. (previously presented) The network interface of claim 1, wherein the set of statistics comprises each of the following: a number of packets received by the interface, a number of bytes received by the interface, a number of packets transmitted by the interface, and a number of bytes transmitted by the interface.

3. (previously presented) The network interface of claim 2, wherein the circuitry comprises circuitry to include a timestamp with the direct memory access transfer of the set of statistics, the timestamp being a time when values of the set of statistics transferred by direct memory access were set by the network interface.

4. (previously presented) The network interface of claim 2, wherein the circuitry comprises circuitry to include a sequence count with the direct memory access transfers of the at least one statistic, the sequence count sequentially numbering successively DMA-ed sets of the statistics.

5. (previously presented) The network interface of claim 1, wherein the set of statistics comprises multiple RMON (Remote Monitoring) statistics.

6. (previously presented) The network interface of claim 1, wherein the circuitry comprises circuitry to initiate direct memory access transfer of received network data.

7. (original) The network interface of claim 1, wherein the network interface comprises a framer.

8. (original) The network interface of claim 7, wherein the network interface comprises a Media Access Controller (MAC).

9. (original) The network interface of claim 1, wherein the network interface comprises a PHY.

10. (previously presented) The network interface of claim 1, further comprising circuitry to configure the circuitry to initiate the direct memory access transfers.

11. (cancelled)

12. (original) The network interface of claim 10, wherein the circuitry to configure comprises at least one register.

13. (currently amended) The network interface of claim 10, wherein the circuitry to configure comprises circuitry to determine said configuration information from said one or more received packets.

14. (currently amended) The network interface of claim 13, wherein the circuitry to determine said configuration information from said one or more received packets comprises circuitry to intercept packets received from the host traveling along said transmit path.

15. (original) The network interface of claim 1, wherein the direct memory access unit comprises circuitry to notify a processor of completion of a transfer.

Claims 16-38. (canceled)